

TITLE OF THE INVENTION

VOLTAGE CONTROLLED OSCILLATOR FOR USE IN PHASE LOCKED LOOP

ABSTRACT OF THE DISCLOSURE

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The present invention provides a clock circuit to produce a Reference Clock Signal used to latch data between first bit stream(s) and second bit stream(s), wherein the number and bit rate of the first bit stream(s) and the second bit stream(s) differ. The VCO generates one of a number of inputs to a PLL within the clock circuit. At a minimum, these inputs
10 include a first bit stream data clock. Additionally, these inputs may further include a Loop Timing Clock Signal, an External Reference Clock Signal, and/or a Reverse Clock Signal for the PLL. The input provided by the VCO make up a VCO Output Signal wherein a filtering circuit that circuit includes a capacitor and a resistor reduces noise contained within the VCO Output Signal.